IN THE CLAIMS

1. (currently amended) An NROM memory transistor comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity type than the remainder of the substrate;

a nanolaminate, high permittivity (high-k), oxidized metal gate dielectric overlying the substrate, the gate dielectric composed of oxide-oxidized Aluminum-oxide; and

a control gate formed on top of the gate ~~dielectric.~~ dielectric;

wherein the oxidized Aluminum has a first concentration of excess Aluminum at a first oxide interface adjacent the substrate and a second concentration of excess Aluminum at a second oxide interface adjacent the control gate; and

wherein the first concentration of excess Aluminum is greater than the second concentration of excess Aluminum.

2. (currently amended) The transistor of claim 1 wherein the oxidized Aluminum of the gate dielectric is ~~a composite oxide – high-k dielectric – oxide nanolaminate gate insulator wherein the high-k dielectric is a charge trapping layer~~ formed by low temperature oxidation of ~~metal~~ Aluminum.

3. (canceled)

4. (original) The transistor of claim 1 wherein the transistor is used in either a NOR-type flash memory structure or a NAND-type flash memory structure.

5. (canceled)

6. (currently amended) The transistor of claim 2 wherein the oxidized Aluminum of the gate dielectric has a larger energy barrier at ~~a high-k dielectric – oxide~~ the second oxide interface than at ~~an oxide – high-k dielectric~~ the first oxide interface.

7 – 48. (canceled)

49. (new) The transistor of claim 1 wherein the plurality of source/drain regions are comprised of an n+ type doped silicon.

50. (new) The transistor of claim 1 wherein the control gate is a polysilicon material.

51. (new) The transistor of claim 1 wherein the substrate is comprised of a p+ type silicon material.

52. (new) An electronic system comprising:
a processor that generates control signals; and
a memory array coupled to the processor, the array comprising a plurality of NROM memory transistors, each NROM memory transistor comprising:
a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity type than the remainder of the substrate;
a nanolaminate, high permittivity (high-k), oxidized metal gate dielectric overlying the substrate, the gate dielectric composed of oxide-oxidized Aluminum-oxide; and
a control gate formed on top of the gate dielectric;
wherein the oxidized Aluminum has a first concentration of excess Aluminum at a first oxide interface adjacent the substrate and a second concentration of excess Aluminum at a second oxide interface adjacent the control gate; and
wherein the first concentration of excess Aluminum is greater than the second concentration of excess Aluminum.

53. (new) The electronic system of claim 52, wherein the oxidized Aluminum of the gate dielectric of at least one memory transistor is formed by low temperature oxidation of Aluminum.

54. (new) The electronic system of claim 52, wherein the memory array has either a NOR-type memory structure or a NAND-type memory structure.

55. (new) The electronic system of claim 52, wherein the oxidized Aluminum of the gate dielectric has a larger energy barrier at the second oxide interface than at the first oxide interface.